

NTD6600N

Power MOSFET 100 V, 12 A, N-Channel, Logic Level DPAK

Features

- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Avalanche Energy Specified
- Logic Level
- Pb-Free Packages are Available

Typical Applications

- PWM Motor Controls
- Power Supplies
- Converters

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|--|-------------------|-------------------|
| Drain-to-Source Voltage | V _{DSS} | 100 | Vdc |
| Drain-to-Source Voltage (R _{GS} = 1.0 MΩ) | V _{DGR} | 100 | Vdc |
| Gate-to-Source Voltage - Continuous | V _{GS} | ± 20 | Vdc |
| Drain Current - Continuous @ T _A = 25°C - Continuous @ T _A = 100°C - Pulsed (Note 3) | I _D I _D I _{DM} | 12 9.0 44 | Adc Adc Apk |
| Total Power Dissipation Derate above 25°C | P _D | 56.6 0.38 | W W/°C |
| Total Power Dissipation @ T _A = 25°C (Note 1) | | 1.76 | W |
| Total Power Dissipation @ T _A = 25°C (Note 2) | | 1.28 | W |
| Operating and Storage Temperature Range | T _J , T _{stg} | -55 to +175 | °C |
| Single Pulse Drain-to-Source Avalanche Energy - Starting T _J = 25°C (V _{DD} = 50 Vdc, V _{GS} = 5.0 Vdc, I _L = 12 Apk, L = 1.0 mH, R _G = 25 Ω) | E _{AS} | 72 | mJ |
| Thermal Resistance - Junction-to-Case - Junction-to-Ambient (Note 1) - Junction-to-Ambient (Note 2) | R _{θJC} R _{θJA} R _{θJA} | 2.65 85 117 | °C/W |
| Maximum Temperature for Soldering Purposes, (1/8" from case for 10 s) | T _L | 260 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

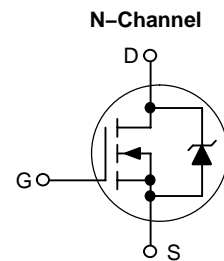
1. When surface mounted to an FR4 board using 0.5 sq in pad size.
2. When surface mounted to an FR4 board using the minimum recommended pad size.
3. Pulse Test: Pulse Width = 10 μs, Duty Cycle = 2%.



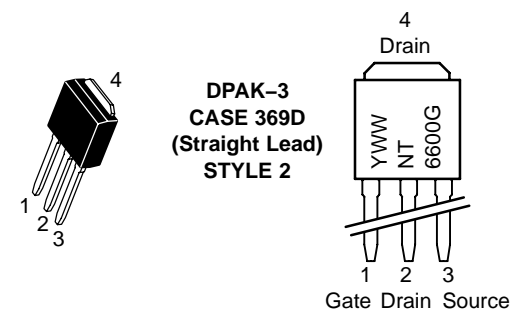
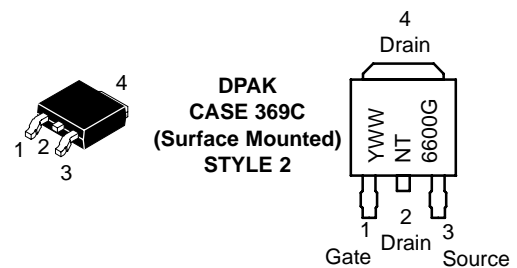
ON Semiconductor®

<http://onsemi.com>

| V _{(BR)DSS} | R _{DS(on)} TYP | I _D MAX |
|----------------------|-------------------------|--------------------|
| 100 V | 118 mΩ @ 5.0 V | 12 A |



MARKING DIAGRAMS



Y = Year
WW = Work Week
NT6600 = Device Code
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

NTD6600N

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

OFF CHARACTERISTICS

| | | | | | |
|--|----------------------|-----|---|-----------|------|
| Drain-to-Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 250 μAdc) | V _{(BR)DSS} | 100 | – | – | Vdc |
| Zero Gate Voltage Drain Current (V _{GS} = 0 Vdc, V _{DS} = 100 Vdc, T _J = 25°C) (V _{GS} = 0 Vdc, V _{DS} = 100 Vdc, T _J = 125°C) | I _{DSS} | – | – | 1.0 10 | μAdc |
| Gate-Body Leakage Current (V _{GS} = ±20 Vdc, V _{DS} = 0) | I _{GSS} | – | – | ±100 | nAdc |

ON CHARACTERISTICS

| | | | | | |
|---|---------------------|----------|-------------|----------|--------------|
| Gate Threshold Voltage V _{DS} = V _{GS} , I _D = 250 μAdc Temperature Coefficient (Negative) | V _{GS(th)} | 1.0 – | 1.5 –4.4 | 2.0 – | Vdc mV/°C |
| Static Drain-to-Source On-State Resistance (V _{GS} = 5.0 Vdc, I _D = 6.0 Adc) | R _{DS(on)} | – | 118 | 146 | mΩ |
| Drain-to-Source On-Voltage (V _{GS} = 5.0 Vdc, I _D = 12 Adc) | V _{DS(on)} | – | 1.5 | 2.2 | Vdc |
| Forward Transconductance (V _{DS} = 10 Vdc, I _D = 6.0 Adc) | g _{FS} | – | 10 | – | mhos |

DYNAMIC CHARACTERISTICS

| | | | | | | |
|------------------------------|---|------------------|---|-----|-----|----|
| Input Capacitance | (V _{DS} = 25 Vdc, V _{GS} = 0 Vdc, f = 1.0 MHz) | C _{iss} | – | 463 | 700 | pF |
| Output Capacitance | | C _{oss} | – | 116 | 225 | |
| Reverse Transfer Capacitance | | C _{rss} | – | 36 | 75 | |

SWITCHING CHARACTERISTICS (Notes 4 & 5)

| | | | | | | |
|-----------------------|--|---------------------|---|------|-----|----|
| Turn-On Delay Time | (V _{DD} = 80 Vdc, I _D = 6.0 Adc, V _{GS} = 5.0 Vdc, R _G = 9.1 Ω) | t _{d(on)} | – | 10.5 | 20 | ns |
| Rise Time | | t _r | – | 75 | 140 | |
| Turn-Off Delay Time | | t _{d(off)} | – | 26 | 40 | |
| Fall Time | | t _f | – | 50 | 90 | |
| Total Gate Charge | (V _{DS} = 80 Vdc, I _D = 6.0 Adc, V _{GS} = 5.0 Vdc) | Q _{tot} | – | 11.3 | 20 | nC |
| Gate-to-Source Charge | | Q _{gs} | – | 1.9 | – | |
| Gate-to-Drain Charge | | Q _{gd} | – | 7.4 | – | |

BODY-DRAIN DIODE RATINGS (Note 4)

| | | | | | | |
|--------------------------------|--|-----------------|---|--------------|----------|-----|
| Diode Forward On-Voltage | (I _S = 12 Adc, V _{GS} = 0 Vdc) (I _S = 12 Adc, V _{GS} = 0 Vdc, T _J = 125°C) | V _{SD} | – | 0.90 0.80 | 1.4 – | Vdc |
| Reverse Recovery Time | (I _S = 12 Adc, V _{GS} = 0 Vdc, di _S /dt = 100 A/μs) | t _{rr} | – | 80 | – | ns |
| | | t _a | – | 50 | – | |
| | | t _b | – | 30 | – | |
| Reverse Recovery Stored Charge | | Q _{RR} | – | 0.240 | – | μC |

4. Indicates Pulse Test: P.W. = 300 μs max, Duty Cycle = 2%.
5. Switching characteristics are independent of operating junction temperature.

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|-------------|---------------------|-----------------------|
| NTD6600N | DPAK | 75 Units/Rail |
| NTD6600N-1 | DPAK-3 | |
| NTD6600N-1G | DPAK-3 (Pb-Free) | |
| NTD6600NT4 | DPAK | 2500 Tape & Reel |
| NTD6600NT4G | DPAK (Pb-Free) | |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTD6600N

TYPICAL CHARACTERISTICS

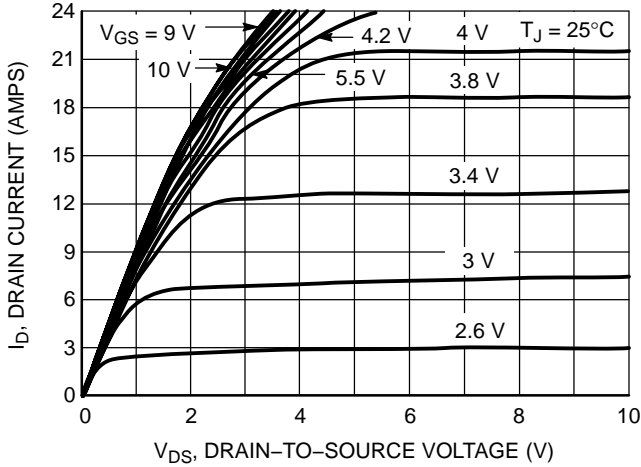


Figure 1. On-Region Characteristics

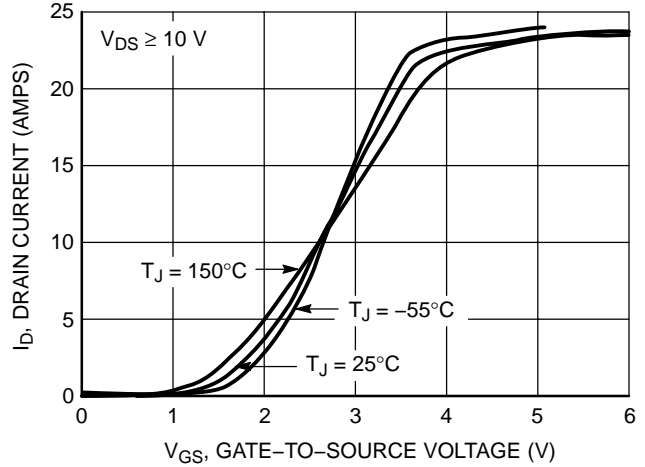


Figure 2. Transfer Characteristics

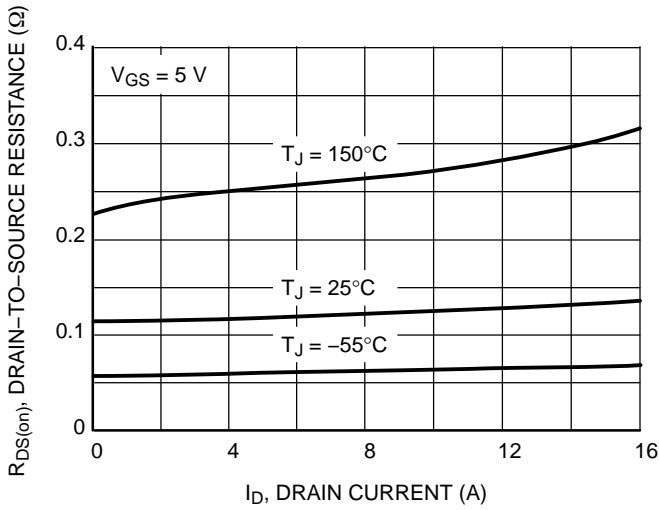


Figure 3. On-Resistance versus Drain Current and Temperature

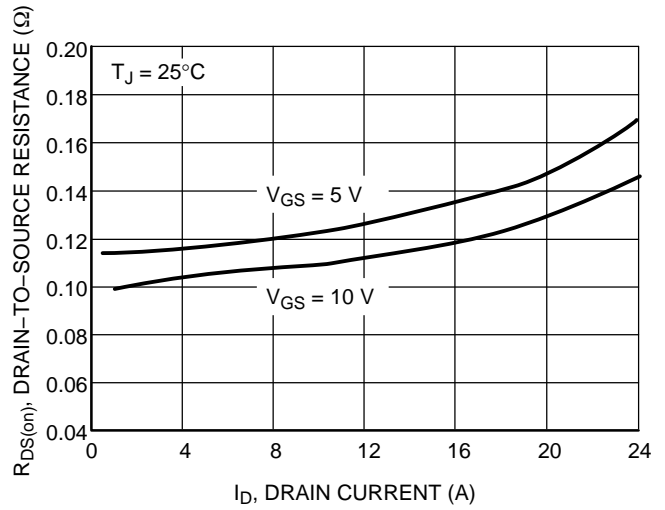


Figure 4. On-Resistance versus Drain Current and Temperature

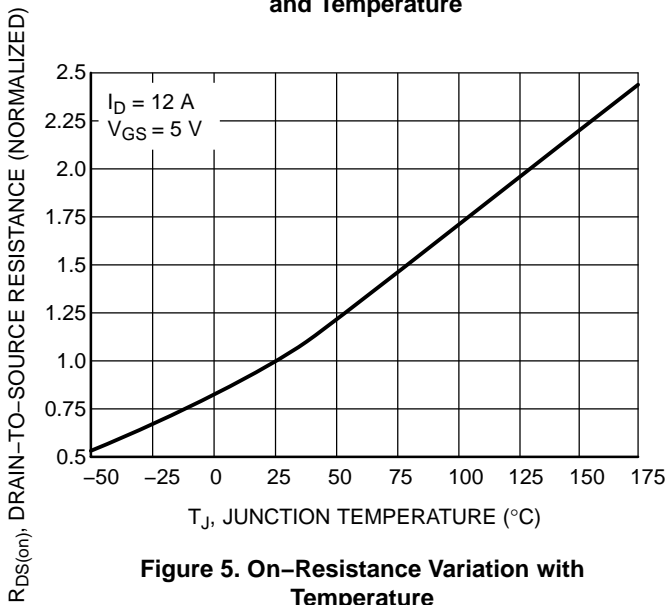


Figure 5. On-Resistance Variation with Temperature

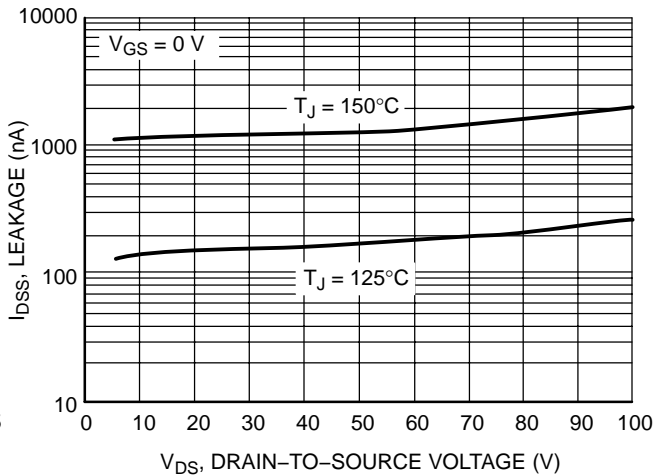


Figure 6. Drain-to-Source Leakage Current versus Voltage

NTD6600N

TYPICAL CHARACTERISTICS

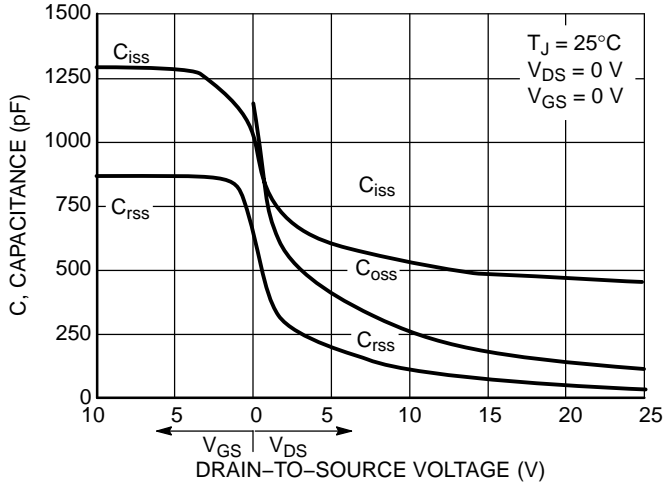


Figure 7. Capacitance Variation

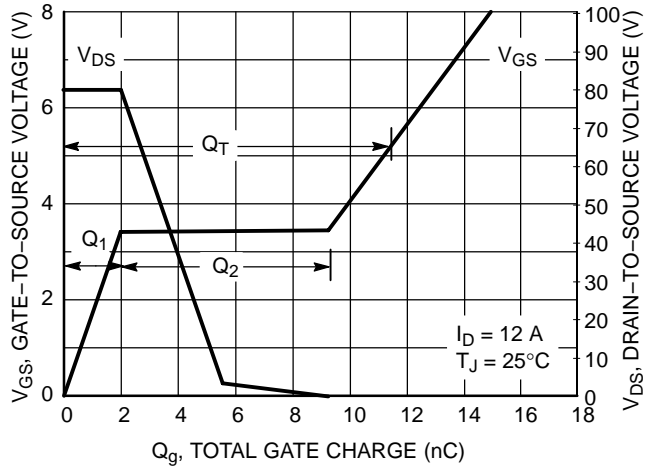


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

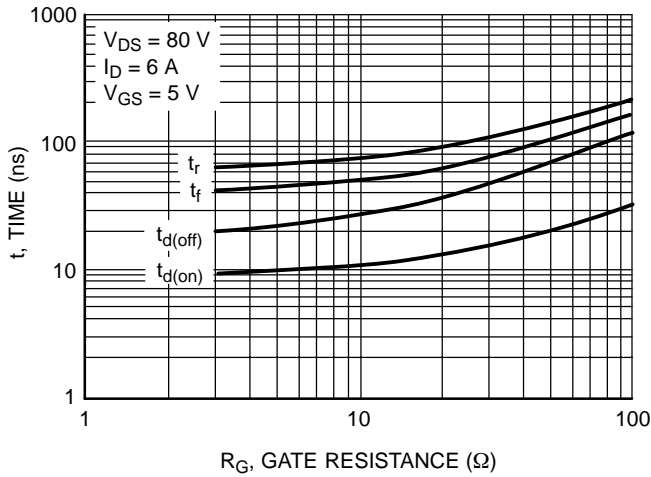


Figure 9. Resistive Switching Time Variation versus Gate Resistance

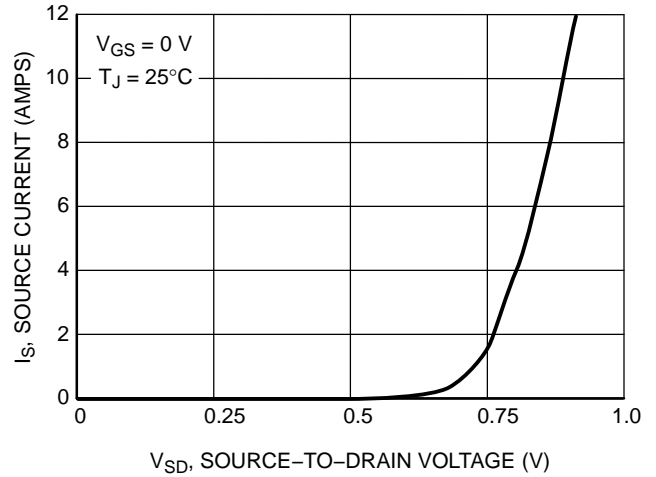


Figure 10. Diode Forward Voltage versus Current

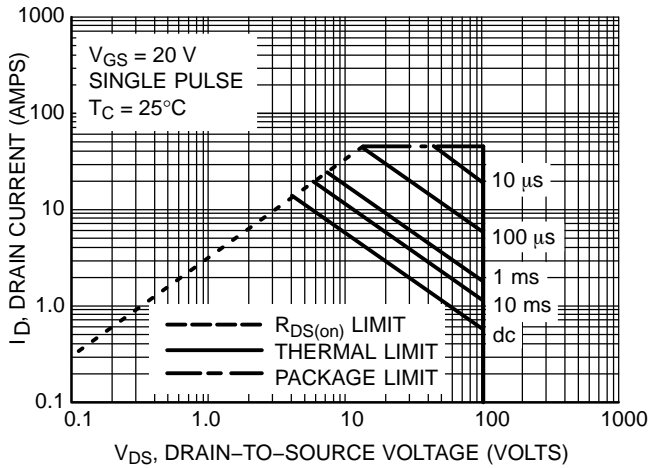


Figure 11. Maximum Rated Forward Biased Safe Operating Area

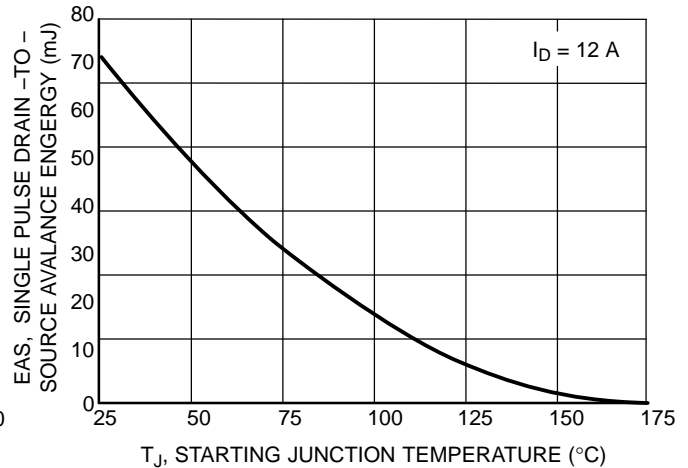
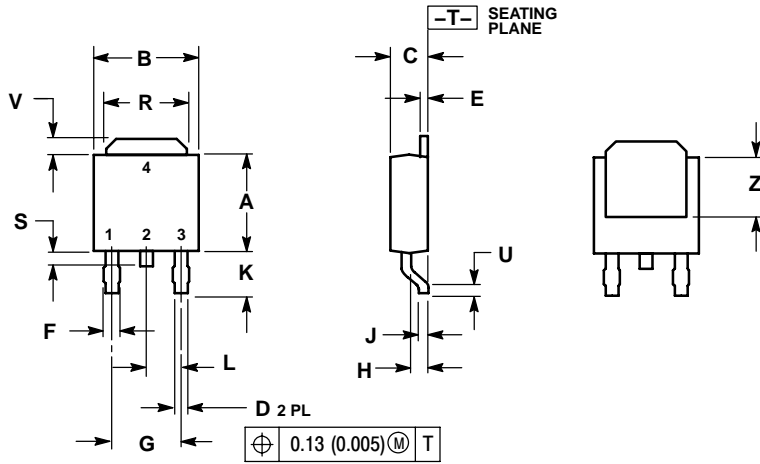


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

NTD6600N

PACKAGE DIMENSIONS

DPAK
CASE 369C-01
ISSUE O

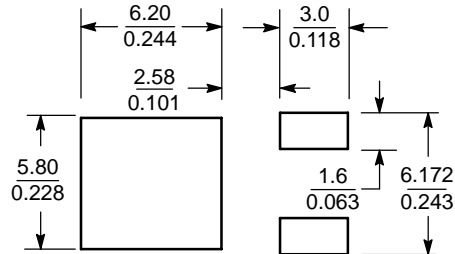


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|----------|-------------|------|
| | MIN | MAX | MIN | MAX |
| A | 0.235 | 0.245 | 5.97 | 6.22 |
| B | 0.250 | 0.265 | 6.35 | 6.73 |
| C | 0.086 | 0.094 | 2.19 | 2.38 |
| D | 0.027 | 0.035 | 0.69 | 0.88 |
| E | 0.018 | 0.023 | 0.46 | 0.58 |
| F | 0.037 | 0.045 | 0.94 | 1.14 |
| G | 0.180 BSC | 4.58 BSC | | |
| H | 0.034 | 0.040 | 0.87 | 1.01 |
| J | 0.018 | 0.023 | 0.46 | 0.58 |
| K | 0.102 | 0.114 | 2.60 | 2.89 |
| L | 0.090 BSC | 2.29 BSC | | |
| R | 0.180 | 0.215 | 4.57 | 5.45 |
| S | 0.025 | 0.040 | 0.63 | 1.01 |
| U | 0.020 | --- | 0.51 | --- |
| V | 0.035 | 0.050 | 0.89 | 1.27 |
| Z | 0.155 | --- | 3.93 | --- |

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

SOLDERING FOOTPRINT*

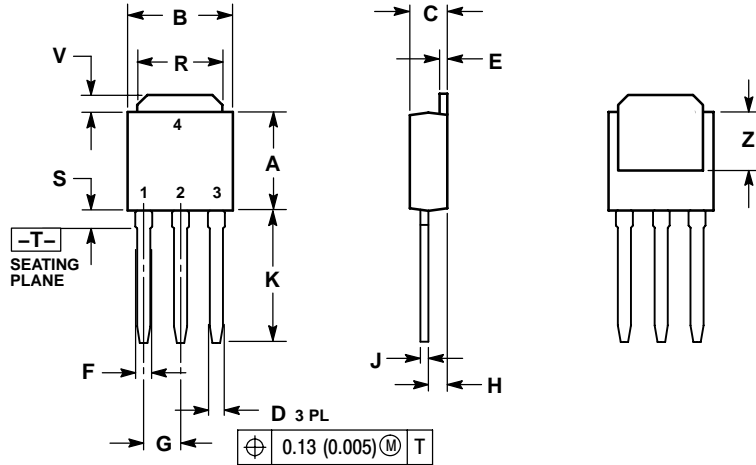


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NTD6600N

PACKAGE DIMENSIONS

DPAK-3
CASE 369D-01
ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|------|
| | MIN | MAX | MIN | MAX |
| A | 0.235 | 0.245 | 5.97 | 6.35 |
| B | 0.250 | 0.265 | 6.35 | 6.73 |
| C | 0.086 | 0.094 | 2.19 | 2.38 |
| D | 0.027 | 0.035 | 0.69 | 0.88 |
| E | 0.018 | 0.023 | 0.46 | 0.58 |
| F | 0.037 | 0.045 | 0.94 | 1.14 |
| G | 0.090 BSC | | 2.29 BSC | |
| H | 0.034 | 0.040 | 0.87 | 1.01 |
| J | 0.018 | 0.023 | 0.46 | 0.58 |
| K | 0.350 | 0.380 | 8.89 | 9.65 |
| R | 0.180 | 0.215 | 4.45 | 5.45 |
| S | 0.025 | 0.040 | 0.63 | 1.01 |
| V | 0.035 | 0.050 | 0.89 | 1.27 |
| Z | 0.155 | --- | 3.93 | --- |

STYLE 2:

- PIN 1. GATE
- DRAIN
- SOURCE
- DRAIN

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative